

FORM HDP-1449 (Based on Form PTO-1449)

**PATENT AND TRADEMARK OFFICE
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Sheet 1 of 2

ATTORNEY DOCKET No.	SERIAL No.
MP0039.C1	10/786,010
APPLICANT	
Roo, Piete	
FILING DATE	GROUP
February 26, 2004	2682

U.S. PATENT DOCUMENTS






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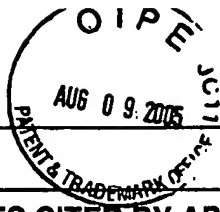
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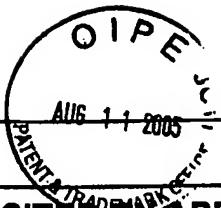
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		FILING DATE 02/26/2004		GROUP Unknown			
DATE SUBMITTED TO USPTO: August 9, 2005							
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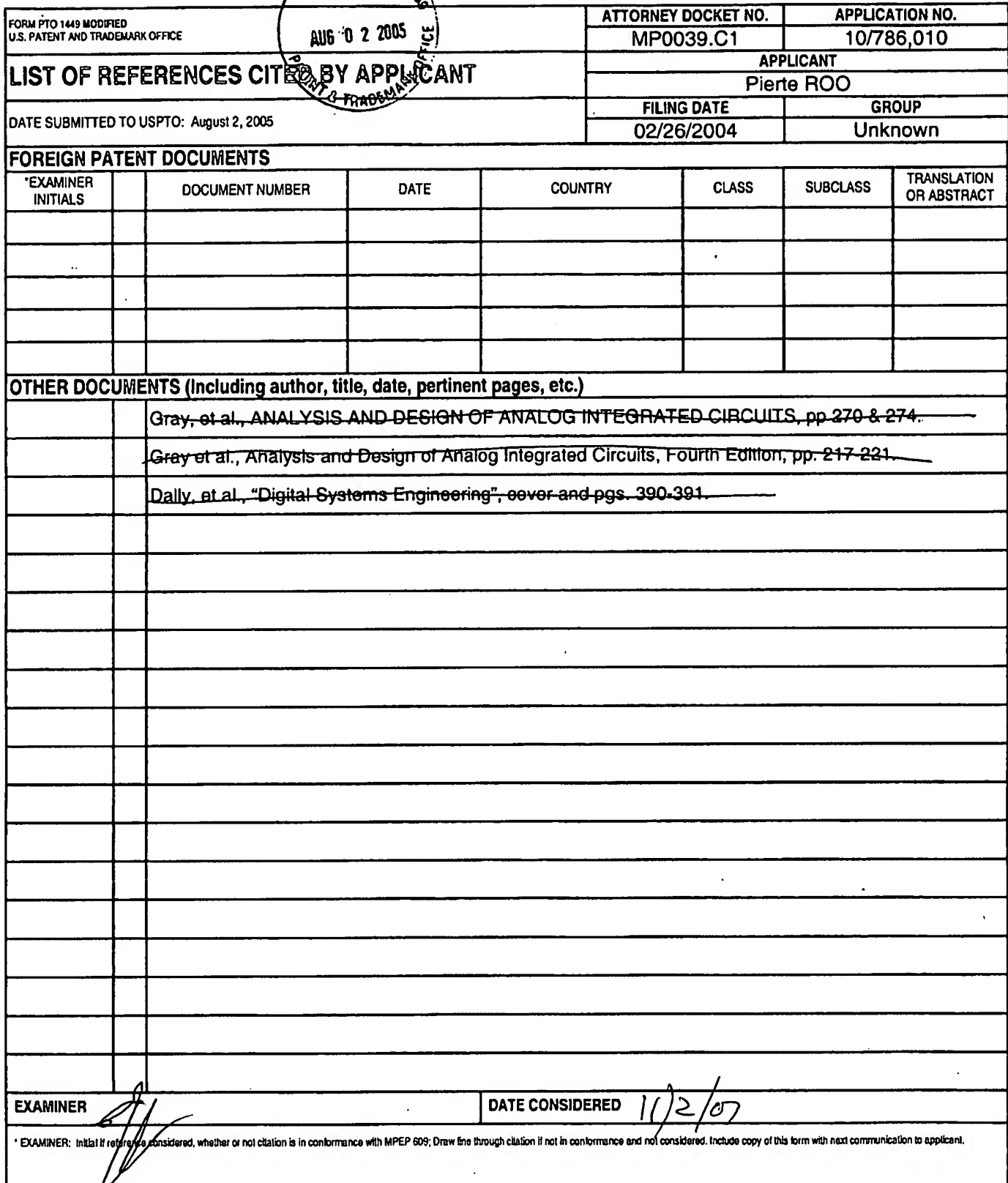
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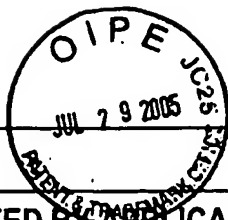
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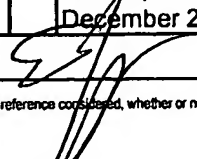
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


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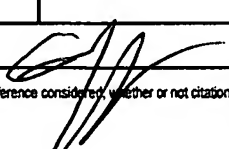
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EXAMINER <i>[Signature]</i>				DATE CONSIDERED <i>11/2/07</i>			
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LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
				FILING DATE 07/12/2005		GROUP Unassigned	
DATE SUBMITTED TO USPTO: July 12, 2005							
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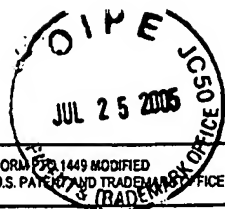
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LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Piete ROO					
		FILING DATE 02/26/2004		GROUP Unknown			
DATE SUBMITTED TO USPTO: July 25, 2005							
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LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Pierre ROO			
				FILING DATE 02/26/2004	GROUP Unknown		
DATE SUBMITTED TO USPTO: July 25, 2005							
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